

sub E3 1
2 164. (Amended) A method of controlling a synchronous memory
3 device by a controller, wherein the memory device includes an array
4 of memory cells and a programmable register, the method of
5 controlling the memory device comprises:

6 issuing a first operation code to the memory device, wherein
7 the first operation code initiates an access of the programmable
8 register in the memory device in order to store a binary value,
9 wherein the binary value is representative of control information;
10 and

11 providing the binary value to the memory device, wherein the
12 memory device stores the binary value in the programmable register
in response to the first operation code.

1 165. (Amended) The method of claim 164 wherein the control
2 information is representative of a number of clock cycles of an
3 external clock signal to transpire before the memory device outputs
4 data in response to a second operation code.

Q2 1 173. (Twice Amended) A synchronous memory device including an
2 array of memory cells, the synchronous memory device comprises:
3 clock receiver circuitry to receive an external clock signal;
4 input receiver circuitry to sample a first operation code
5 synchronously with respect to a transition of the external clock
6 signal; and

7 a programmable register to store a binary value that is
8 representative of control information, wherein the memory device
9 stores the binary value in the programmable register in response to
10 the first operation code.

1 174. (Amended) The memory device of claim 173 wherein the
2 control information is representative of a number of clock cycles
3 of the external clock signal to transpire before the memory device
4 outputs data and wherein the memory device outputs data in response
5 to a second operation code.

1 183. (Amended) The method of claim 164 wherein the first
2 operation code is issued to the memory device via an external bus.

Kindly ADD the following claims:

1 193. (New) The method of claim 164 wherein the control
2 information includes a device type identifier.

1 194. (New) The method of claim 164 wherein the control
2 information identifies a location of a defective portion of the
3 array of memory cells.

1 195. (New) The method of claim 164 wherein the control
2 information identifies a range of addressable locations of the
3 array of memory cells.

1 196. (New) The method of claim 164 wherein the control
2 information includes a device identification value to identify the
3 memory device uniquely among a plurality of memory devices.

4 197. (New) The memory device of claim 173 wherein the control
5 information includes a device identifier.

1 198. (New) The memory device of claim 173 wherein the control
2 information identifies a location of a defective portion of the
3 array of memory cells.

1 199. (New) The memory device of claim 173 wherein the control
2 information identifies a range of addressable locations of the
3 array of memory cells.

200. (New) The memory device of claim 173 wherein the control information includes a device identification value to identify the memory device uniquely among a plurality of memory devices.

201. (New) The memory device of claim 173 further including a plurality of registers, wherein the programmable register is included in the plurality of registers, and wherein the plurality of registers further includes at least one of:

a first register to store a value that identifies the memory device uniquely among a plurality of memory devices;

a second register to store a value that identifies a range of addressable locations of the array of memory cells; and

a third register to store a value that identifies a location of a defective portion of the array of memory cells.